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Self-aligned patterning method of poly(aniline) for organic field-effect transistor gate electrode

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ABSTRACT

We present a new manufacturing method for the bottom-gate type organic field-effect transistor (OFET) having a self-aligned gate electrode based on conducting poly(aniline). This method utilizes the possibility to turn the insulating emeraldine base (PANI-EB) form of poly(aniline) into the conducting emeraldine salt (PANI-ES) form by using UV exposure and photoacid generator (PAG) material. When the source–drain electrodes are used as the mask layer in the UV exposure step an optimal alignment between the gate electrode and source–drain electrodes can be reached, and the parasitic capacitance of the transistor can be minimized. We anticipate that the proposed concept also simplifies the fabrication of the transistors since no additional processing of the photoresist layers is needed to pattern the gate electrode or the gate insulator layer.

1. Introduction

For many applications of organic semiconductors it is desirable to pattern one or several organic layers [1–4]. One example is the organic field-effect transistor (OFET), which typically contains the following separate layers: source–drain (S–D) electrodes, semiconductor layer, gate insulator layer and the gate (G) electrode [5–8]. The area separating the source and drain, filled with the semiconductor material, defines the transistor channel. The channel dimensions have a strong effect on the transistor performance. To increase the bandwidth and thereby the application areas of OFETs, it is required to increase the charge carrier mobility in the semiconductor material and decrease the channel length. In addition, the parasitic gate capacitance area, i.e. the overlapping area between the gate and source–drain electrodes, should be minimized [9,10]. However, minimizing parasitic capacitances is not straightforward in a roll-to-roll or printing based fabrication process. There are two main reasons for this. First, going for shorter transistor channels means that the gate pattern should have as far as possible the same (small) dimensions as the channel. Especially in the top-gate OFET configuration, this is technologically very challenging. Second, aligning the gate pattern accurately to the transistor channel is limited by the modest registration accuracy of the typical printing equipment. Various effects such as clearances and wearing of mechanical parts, tensions to the web and temperature related stretching result in limited registration accuracy that can be as low as several hundred micrometers. To solve the process limitations in a roll-to-roll fabrication, it would be preferable to find a way, in which the gate and the channel in an OFET are automatically aligned (self-aligned) in respect to each other during the transistor fabrication. Several different methods have been presented to solve this alignment problem [11–18]. One favorable concept is to use the gate electrode layer as the shadow mask to define the source–drain electrodes by a back surface substrate exposure [11,13,15,18]. This sets the requirement of transparency to the substrate material.

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The approach taken in this study was to utilize the doping properties of non-conducting poly(aniline) (PANI) thin film in the realization of a self-aligned fabrication concept for OFETs. Previously, intrinsically conducting polymer poly(aniline) has already been used in different parts of OFETs [19,20] and especially in all-polymer versions [21,22], where simple processing of several overlapping layers e.g. by printing is preferred. As known the conductivity level of poly(aniline) can be varied by several decades through doping and dedoping processes, and so it is possible to pattern conductive poly(aniline) thin films with standard photolithography [23]. Alternatively, a photoacid generator (PAG) material can be mixed into the insulating emeraldine base form of PANI, and upon UV irradiation the PAG produces a bronsted acid, which turns the insulating base form of PANI into the conducting salt form [24–26]. In this work we show that it is possible to use the source–drain electrodes as the UV mask layer to pattern the gate electrode into the insulating PANI-EB thin film located under the gate insulator layer and to get an optimal self-alignment between the electrode layers. No requirement for the transparency of the substrate is set as a bottom-gate structure is used.

2. Materials and methods

2.1. Materials

1.5 wt% PANI-EB solution in *N*-methyl-2-pyrrolidone (NMP) was prepared from PANI-EB purchased from Panipol Ltd (Finland) (Fig. 1a). 1-naphthyl diphenyl sulfonium triflate ($NaphPh_2SOTf$) type onium salt (Sigma–Aldrich) was used as the photoacid generator (Fig. 1b). Several solutions with different concentrations of the PAG material were prepared in order to find the PAG/PANI ratio that produced the highest conductivity in UV exposed films. The reported results were achieved by adding 33 mol% (compared to the structural unit of PANI) of 1-naphthyl diphenyl sulfonium triflate to the PANI/NMP solution. The solution was stirred for 30 min and then filtered (pore size 1 μm). The gate insulator solution was prepared by dissolving 8.5 wt% poly(methyl methacrylate) (PMMA) (M_W 120,000 g/mol, Sigma–Aldrich) in toluene and the solution was filtered (pore size 0.45 μm).

Alternatively 12.6 wt% PANI-ES dispersion in toluene (PANI-T from Panipol Ltd) was used for preparing the patterned PANI films. For dedoping the films 10 wt% sodium hydroxide (NaOH) was dissolved in deionized water (DIW). $NaphPh_2SOTf$ was used as a separate solution of 10 wt% in ethanol (EtOH).

2.2. Sample preparation

Golden contact pads (thickness 40 nm) for the gate electrodes were first evaporated through a shadow mask on 125 μm thick polyethylene terephthalate (PET) substrate film (Melinex 538 from DuPont Teijin Films). The contact pads mimicked the contact to the possible circuit, to which the transistor would be contacted. The self-alignment procedure reported in this paper serves as a means to overcome the registration accuracy limitations of R2R processing equipment. For the alignment of for example the transistors to the rest of the circuit the available R2R registration accuracy is sufficient in most cases. Then the substrate was treated with oxygen plasma (0.3 mbar, 10 min) in a plasma etcher (Nano, Diener Electronic) to promote adhesion of the PANI-EB/$NaphPh_2SOTf$ in NMP solution. The PANI-EB/$NaphPh_2SOTf$ solution was spin-coated (500 rpm, 20 s) on the substrate film and dried in a vacuum oven in room temperature for 16 h.

The gate insulator layer was made by spin-coating the 8.5 wt% PMMA in toluene solution (1000 rpm, 5 s) on the PANI-EB/$NaphPh_2SOTf$ film and then the samples were dried on a hotplate (60 °C, 2 min) and crosslinked (130 °C, 50 min) in N_2 atmosphere.

Golden source and drain electrodes (thickness 80 nm) were evaporated through a shadow mask on the gate insulator layer. The channel length (L) was 50 μm and the channel width (W) was 2 mm. The samples were then exposed to UV radiation (LV204 UV Exposure Unit, Mega Electronics Ltd, 15 W) for an optimized time of 45 min through the source and drain electrodes and having a coarse UV mask around the gate areas (Figs. 2b and 3a). Finally, the samples were treated in oxygen plasma (0.3 mbar, 6 min) to promote the adhesion of non-commercial *p*-type organic semiconductor solution (2 wt% in dichlorobenzene), which was spin-coated on top of the transistor structure (1000 rpm, 20 s) and dried in room atmosphere.

Another method for preparing patternable PANI films was also tested. Conducting PANI-T solution was spin-coated on the PET substrate and dedoped by pipetting an excess amount of 10% NaOH solution on top of the dried film. The excess NaOH was washed away by spinning the

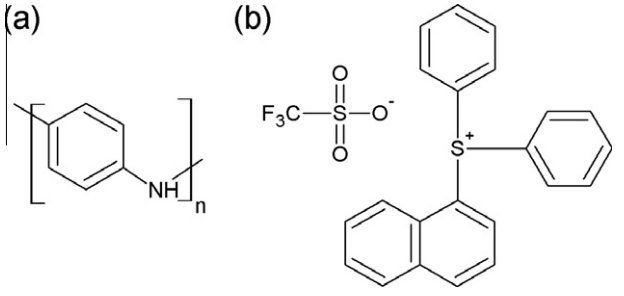

Fig. 1. Chemical structures of (a) poly(aniline) in its emeraldine base (PANI-EB) state and (b) 1-naphthyl diphenyl sulfonium triflate.

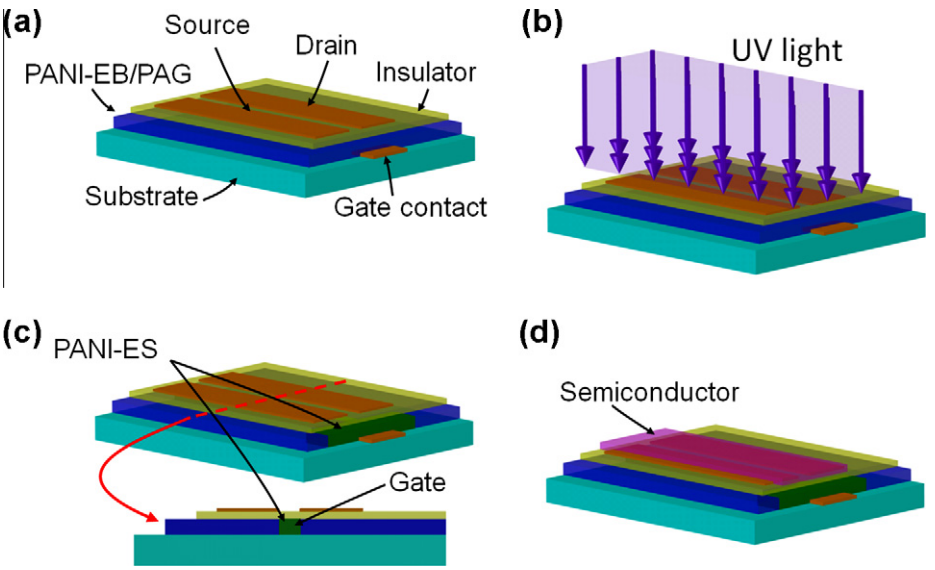

Fig. 2. Fabrication procedure of the self-aligned bottom-gate type transistors having conducting poly(aniline) as the gate electrode. (a) The gate insulator layer and source-drain (S-D) electrodes manufactured on top of the PANI-EB/photoacid generator (PAG) layer, (b) exposure by UV radiation through source-drain electrodes causes the decomposition of 1-naphthyl diphenyl sulfonium triflate salt, (c) in the green area protonic acid has turned the insulating PANI-EB into the conducting PANI-ES form, (d) the organic semiconductor layer is spin-coated on top of the S-D electrode layer.

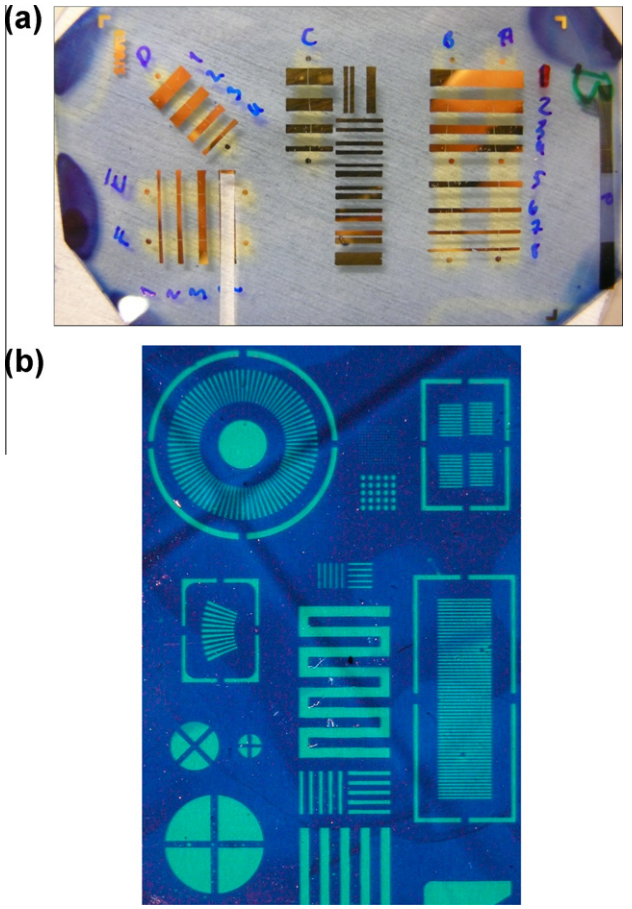

Fig. 3. (a) PANI-EB/1-naphthyl diphenyl sulfonium triflate salt film and (b) dedoped PANI-T/1-naphthyl diphenyl sulfonium triflate salt film showing green areas that have been exposed to UV radiation. The smallest irradiated patterns are 0.001" diameter holes. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

sample (1000 rpm) and pipetting first EtOH and then DIW on the spinning sample. Finally the $NaphPh_2SOTf$ solution (10 wt% in EtOH) was spin-coated (1000 rpm) on top of the dedoped PANI film. These samples were patterned using a separate photomask (45 min in LV204 UV Exposure Unit). After the UV exposure the excess PAG material was washed away by rinsing with isopropyl alcohol (IPA).

2.3. Electrical measurements

The dc conductivity measurements were made to detect the difference in the square resistance R_s [Ω/sq] of the insulating PANI-EB form and the conducting PANI-ES form of poly(aniline). I–V curves were measured with Keithley 4200-SCS (two-probe configuration) from spin-coated thin film samples with evaporated golden electrodes over a 50 μm gap. Variable electrode widths were used and measurements conducted in 8 separate points over a 15 cm^2 film area in order to examine the uniformity of the PANI/PAG film. The square resistance R_s [Ω/sq] was calculated from the linear I–V curves measured from −30 to 30 V for the non-exposed (PANI-EB) samples and from −15 to 15 V for the exposed (PANI-ES) samples. Fabricated bottom-gate type OFETs were measured in normal room atmosphere and temperature using a Keithley 4200-SCS Semiconductor Characterization Analyzer.

2.4. Film thickness

The thicknesses of the insulating and conducting poly(aniline) thin films were measured with a Surface Profiler (Dektak 150, Veeco) from dried films.

2.5. Transistor fabrication

The fabrication procedure of the self-aligned transistors shown in Fig. 2 includes the following steps: (1) coating or printing the PANI-EB/photoacid generator (PAG) mixture on top of the substrate film, (2) coating or printing the gate insulator layer on top of the PANI-EB/photoacid generator layer, (3) manufacturing the source–drain (S–D) electrodes on top of the gate insulator layer (Fig. 2a), (4) exposure by UV radiation through S–D electrodes to pattern the self-aligned gate electrode (Fig. 2b and c). Finally the organic semiconductor layer is spin-coated on top of the S–D electrode layer (Fig. 2d).

3. Results and discussion

The square resistance of the spin-coated poly(aniline)/1-naphthyl diphenyl sulfonium triflate salt films was measured before and after the UV exposure to find out the difference in the conductivity level of the undoped PANI-EB/onium salt mixture and the poly(aniline) doped by the decomposed onium salt. Angelopoulos et al. have reported the conductivity value of 0.1 S/cm using diphenyliodonium hexafluoroantimonate type onium salt as the PAG [24]. For the films prepared from the PANI-EB/$NaphPh_2SOTf$ in NMP solution, similar values for the conductivity were achieved as the thickness of the films was ca. 100–150 nm. This proves that 1-naphthyl diphenyl sulfonium triflate is a good choice for a PAG material to protonate insulating PANI films in solid form. The results of the square resistance measurements of the PANI-EB/$NaphPh_2SOTf$ films prepared from NMP solution are presented in Table 1. Exposed (PANI-ES) films showed a nearly linear relationship between electrode width and measured resistance. Therefore, the calculated square resistance values are very close to each other, and it can be deduced that the films are uniform. For the non-exposed (PANI-EB) films the resistance values are too great to be measured with similar accuracy and hence, the deviation is higher. However, the UV exposure is shown to cause a several decade decrease in the square resistance.

More conductive films of PANI/$NaphPh_2SOTf$ were achieved by preparing the films from the toluene-based PANI-T solution following the previously described procedure. When using the PANI-T solution there were no problems with the adhesion and therefore the film thickness could be adjusted by altering the spinning speed. PANI films prepared by the spinning speed of 4000 rpm were ca. 200 nm thick (measured after the UV exposure and washing away the excess PAG). The square resistance of these films was on the order of 10^{10} Ω before the UV exposure (PANI-EB form) and on the order of 10^4 Ω after the exposure (PANI-ES form). However, there were problems with producing films with uniform quality since $NaphPh_2SOTf$ was not spread evenly due to the spin coating method and the exposed films had a marble-like pattern. In addition, the remaining PAG layer under the dielectric would have risked the stability and the performance of the transistor when using a bottom gate structure. Therefore transistor structures using the PANI films prepared from PANI-T were not made.

In visual inspection the unexposed areas of PANI-EB/1-naphthyl diphenyl sulfonium triflate salt films are blue in color, while after the UV exposure for 45 min the exposed regions have turned green (Fig. 3a), which indicates doping of PANI. The color change can best be seen in thicker films prepared from the PANI-T solution (Fig. 3b).

In the transistor structures capacitance between gate and the drain–source electrodes was not trivial to measure, as the large square resistance of the PANI gate added an extra series term in the measurement [27]. Still, some rough values were obtained. The capacitance of the self-aligned structure was smaller than 5 pF, which is in the same range as the channel capacitance. The similar overlapped structure would have an additional capacitance on the order of 200 pF. Also the leakage current from the source and drain electrodes to the gate was measured before the semiconductor deposition. Even at high voltages (200 V) the current was smaller than could be measured reliably (<1 nA), indicating that the self-aligned gate is formed only to the areas outside the shadowing effect of the source and drain electrodes. If there would have been an overlapping bottom electrode, the dielectric layer would not have withstood the high voltage used. After the semiconductor deposition the gate leakage current increased remarkably. Thicker or better dielectric or a smoother PANI surface could decrease the gate leaking.

The transistor measurement took place after drying of the final semiconductor layer. In order to verify

Table 1
The measured resistances before (R_{EB}) and after the UV exposure (R_{ES}) and the corresponding square resistances ($R_{s,EB}$ and $R_{s,ES}$). W indicates the width of the electrodes and L is the length of the gap.

Pattern	R_{EB}/Ω	R_{ES}/Ω	$W/\mu m$	$L/\mu m$	$R_{s,EB}/\Omega$	$R_{s,ES}/\Omega$
1	2.25E+07	3.86E+04	2200	50	9.90E+08	1.70E+06
2	3.88E+09	4.07E+04	1600	50	1.24E+11	1.30E+06
3	2.54E+10	5.40E+04	1200	50	6.10E+11	1.30E+06
4	3.90E+09	6.44E+04	1000	50	7.80E+10	1.29E+06
5	1.82E+11	8.97E+04	600	50	2.18E+12	1.08E+06
6	1.28E+10	1.15E+05	400	50	1.02E+11	9.20E+05
7	6.35E+10	5.70E+04	1100	50	1.40E+12	1.25E+06
8	8.72E+10	6.23E+04	1000	50	1.74E+12	1.25E+06
Average					7.79E+11	1.26E+06
Standard deviation					8.13E+11	2.08E+05

semiconductor material stability transistor characteristics were measured after 1 and 15 h, and found similar. The measurement showed a typical OFET behavior (Figs. 4 and 5). The transfer curve (Fig. 4b) shows no hysteresis, which means that there is not any special interface trapping problems on either side of the dielectric layer [28]. The square root of drain current versus gate voltage in Fig. 4b shows a straight line, giving *field effect mobility* 0.008 cm^2/Vs and threshold voltage close to zero. Values are comparable to ones achieved with other transistor geometries with the same materials. Fig. 5 shows the drain current and considerably large gate leaking current. The *On/Off* ratio measured between −20 and 0 V is only 44, which is partly due to gate leakage and partly due to a positive *Turn On* voltage.

The high gate resistance could slow the transistor operation considerably. According to Jung et al. [27] the charge response time in the channel is proportional to the sum of the channel and the gate resistance. Normally the gate resistance is very small and could be neglected, but for these transistors the effective channel resistance is in the same order of magnitude as the gate resistance ($\sim 10^6$–$10^7\ \Omega$). For more usable transistors with much wider (W) channels the gate resistance would start to dominate as the $R_{Channel} \sim 1/W$ and $R_{Gate} \sim W$. On the whole measurement results show that this special UV exposure technique can be used to form a self-aligned gate electrode. These mediocre transistor characteristics do not show the full

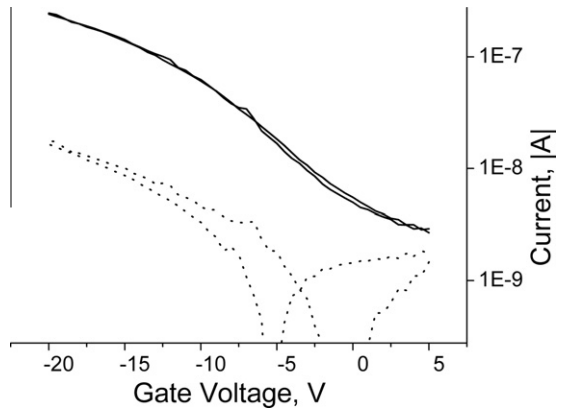

Fig. 5. Drain (solid) and gate (dashed) current on logarithmic scale. There is a considerable gate leaking current.

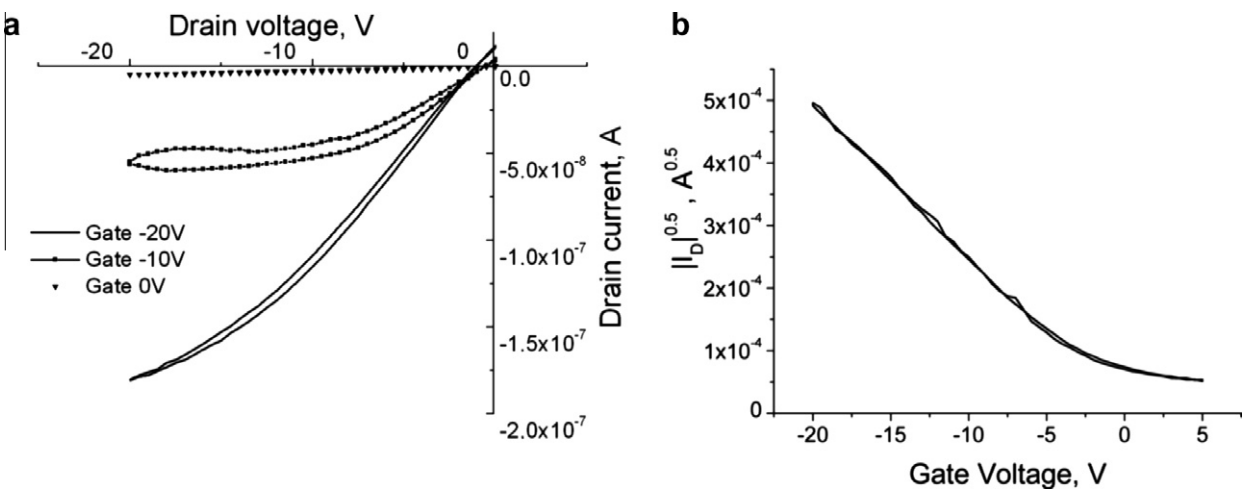

Fig. 4. (a) Output characteristics and (b) saturation drain current versus gate voltage characteristics of a transistor made with self-aligned PANI gate. Plots show that there is some hysteresis in the output curve but not in the transfer curve. The channel length (L) was 50 μm and the channel width (W) was 2 mm.

potentiality of the method. The dielectric and semiconductor layers were not optimized, but still proved the concept well.

The presented transistor fabrication process can be carried out in normal room atmosphere and lighting. The PAG material used does react to natural light over time, but so slowly that it does not require any special manufacturing conditions. However, to secure the stability of the transistor it is advisable to use a barrier layer or encapsulation to protect the PANI/PAG layer and semiconductor from ambient light.

As described before, a more conductive UV patternable gate electrode could be manufactured from the dedoped toluene-based PANI-ES film. However, it was also mentioned that if the transistor would be made by the procedure presented, the remaining layer of PAG material between PANI and the gate insulator films could cause stability problems. This is why a top-gate transistor structure is a better choice than the bottom-gate geometry. In this case source and drain electrodes as well as semiconductor and gate insulator layers are first fabricated on a transparent substrate. Then the PANI-T solution is coated on top, dedoped and covered with the PAG material. Next the gate electrode is made into the insulating PANI film by UV exposure through the substrate. Finally, the excess PAG is washed away with alcohol and thus the stability of the transistor is improved. This procedure of course requires UV stable semiconductor material and needs more research.

4. Conclusions

We have presented a novel method to fabricate a bottom-gate type organic field-effect transistor having a self-aligned gate electrode based on conducting poly(aniline). In this method insulating PANI-EB/1-naphthyl diphenyl sulfonium triflate thin film is exposed to UV radiation through the drain–source electrode layer and turned into conducting PANI-ES form to pattern the self-aligned gate electrode of the OFET. Transistors made by this method showed that this technique can be used to form a self-aligned gate and the PANI-EB/salt combination is compatible with a typical OFET dielectric. We expect that the concept can be used to generate also other UV patternable structures.

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